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EXAMINER	
TAYLOR, EARL N	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,020	GLASSE ET AL.	
	Examiner	Art Unit	
	EARL N. TAYLOR	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15* is/are rejected.

7)☒ Claim(s) *16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of claims 8-17 is withdrawn in view of the newly discovered reference(s) to Nakajima (U.S. Patent 6,420,758 B1). Rejections based on the newly cited reference(s) follow.

Claim Objections

Claims 10-12 are objected to because of the following informalities:

Claim 10 recites "the conductive material" and should read --the layer of conductive material--.

Claim 11 recites "the layer" and should read --the layer of conductive material--.

Claim 12 recites "said layer" and should read --said layer of conductive material-- or --the layer of conductive material--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

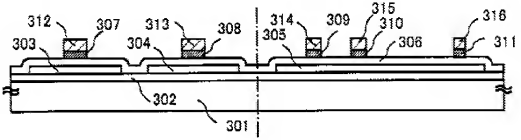
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima (U.S. Patent 6,420,758 B1) hereinafter referred to as "Nakajima".

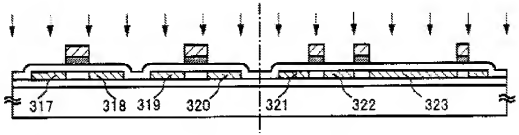
Referring to Claim 8, Nakajima teaches, in Fig. 3A-3C and 16A-16D for example, a method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

FIG. 3A



(a) providing a gate (307 and 312) separated from a polycrystalline silicon layer (303) by an insulating layer (306) (Fig. 3A);

FIG. 3B



(b) implanting a dopant (317 and 318) into the polycrystalline silicon layer (303) using the gate (307 and 312) as a mask (Fig. 3B);

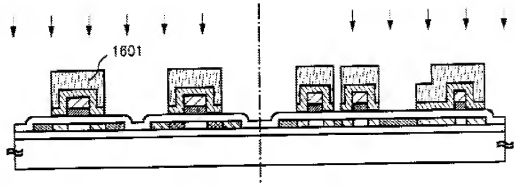


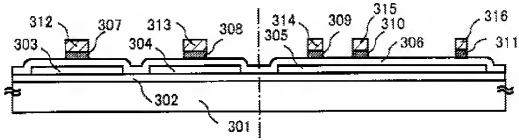
FIG. 16A

(c) forming a spacer (1603; Fig. 16A-16D) after step (b) adjacent to the gate (307 and 312) that comprises a conductive region which overlies the polycrystalline silicon layer (303) and extends along the gate (307 and 312) side wall, comprising depositing a layer of conductive material (second gate) over the polycrystalline silicon layer (303) and the gate (307 and 312), and selectively etching the deposited layer of conductive material (second gate) to form the spacer (1603) with a first portion overlying the polycrystalline silicon layer (303) and a second portion extending along on the side wall of the gate (307 and 312), wherein the layer of conductive material (second gate) has a thickness less than that of the gate (307 and 312); and

(d) implanting a dopant into the polycrystalline silicon layer (303) using the gate (307 and 312) and the spacer (second gate) as a mask to form a source or drain region, such that the spacer (second gate) overlies an LDD region in the polycrystalline silicon layer (303) between the source or drain region and the channel (Col. 9, Line 8 to Col. 11, Line 9 and Col. 17, Lines 28-64).

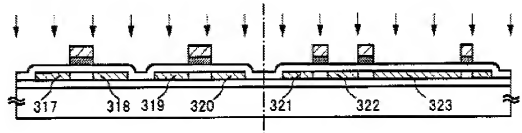
Referring to Claim 13, Nakajima teaches a method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

FIG. 3A



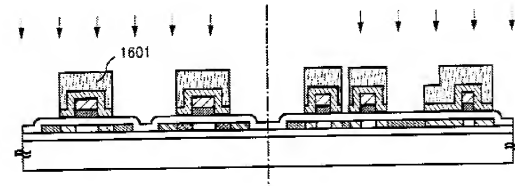
(a) providing a gate (307 and 312) separated from a polycrystalline silicon layer (303) by an insulating layer (306);

FIG. 3B



(b) implanting a dopant into the polycrystalline silicon layer (303) using the gate (307 and 312) as a mask;

FIG. 16A



(c) forming a spacer layer (1603; Fig. 16D) after step (b) adjacent to the gate (307 and 312) that comprises a conductive region which overlies the polycrystalline

silicon layer (303) and extends along the gate (307 and 312) side wall, comprising depositing a layer of conductive material (second gate) over the polycrystalline silicon layer (303) and the gate (307 and 312), and selectively etching the deposited layer of conductive material (second gate) to form the spacer (1603) with a first portion overlying the polycrystalline silicon layer (303) and a second portion extending along on the side wall of the gate (307 and 312), wherein the selective etching of the conductive layer (second gate) is carried out by forming a fillet (1601) over the first portion thereof, and selectively etching the conductive layer (1603) where not protected by the fillet (1601); and

(d) implanting a dopant into the polycrystalline silicon layer (303) using the gate (307 and 312) and the spacer (1603) as a mask to form a source or drain region, such that the spacer (1603) overlies an LDD region in the polycrystalline silicon layer (303) between the source or drain region and the channel (Col. 9, Line 8 to Col. 11, Line 9 and Col. 17, Lines 28-64).

Referring to Claim 9, Nakajima further teaches depositing the layer of conductive material (1603) to a thickness which is less than that of the gate (307 and 312).

Referring to Claim 14, Nakajima further teaches depositing a further layer (1601) on said conductive layer (second gate), and selectively etching the further layer (1601) to form the fillet therefrom.

Referring to Claim 15, Nakajima further teaches depositing the further layer (1601) as a conformal layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-13 are rejected under 35 U.S.C. 103(a) as being anticipated by Takehashi et al. (PCT Publication No. WO00/54339). The English equivalent, Takehashi et al. (U.S. Patent 6,624, 473 B1) is used hereinafter and is referred to as "Takehashi".

Referring to Claims 8 and 10-12, Takehashi teaches, in Fig. 11, 12 and 13 for example, a method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate (42) separated from a polycrystalline silicon layer (1) by an insulating layer (2) (Fig. 12e and 12f);

(b) implanting a dopant (P+) into the polycrystalline silicon layer (1) using the gate (42) as a mask (Fig. 12g);

(c) forming a spacer (43) after step (b) adjacent to the gate (42) that comprises a conductive region which overlies the polycrystalline silicon layer (1) and extends along the gate (42) side wall, comprising depositing a layer of conductive material (430) over the polycrystalline silicon layer (1) and the gate (42), and selectively etching the

deposited layer of conductive material (430) to form the spacer (43) with a first portion overlying the polycrystalline silicon layer (1) and a second portion extending along on the side wall of the gate (42); and

(d) implanting a dopant (impurity ions) into the polycrystalline silicon layer (1) using the gate (42) and the spacer (43) as a mask to form a source or drain region (150 and 160), such that the spacer (43) overlies an LDD region (152 and 162) in the polycrystalline silicon layer (1) between the source or drain region (150 and 162) and the channel (170) but does not explicitly state in this embodiment wherein the layer of conductive material (43) has a thickness less than that of the gate (42). However, Takehashi teaches:

> Regarding the material of the two-staged gate electrode, the density of the material of the upper gate electrode 42 is desired to be higher than that of the lower gate electrode 43 from the standpoint of the height of gate electrode (if too high, however, such inconvenience would arise as too thick a gate insulator) and masking effect. More concretely, the material of the lower gate electrode 42 will preferably be Al, Al/Ti, Al/Zr/Ti, while that of the upper gate electrode 43 will preferably be Ta, Cr, Mo, etc (Col. 18, Lines 55-63).
>
> As has been described earlier, the density of the material for the upper gate electrode should be higher than that for the lower gate electrode in due consideration of the necessity of perfect masking capacity at the time of the second doping (Col. 20, Lines 10-13).
>
> The upper gate electrode film 420 was made to accumulate on the SiO.sub.2 film. Although this embodiment used the ITO film as shaped by sputtering method (film thickness: about 500Å), we may safely use such metallic films as aluminum, tantalum, titanium, molybdenum, tungsten, and zirconium, their alloy-based films, and such conductive oxide films as ITO. In these cases, however, the optimal film thickness should be determined individually in due consideration of the doping in the LDD area using this lower electrode as mask in the subsequent process. Further, since the stopping power of the ions (capacity to interfere with the passing of accelerated ions) to be doped depends on the film material, the optimal film thickness is naturally dependent also on the material composition of the film. (c) Formed on the lower gate electrode film 420 was a

tantalum film of 2000 Å in thickness as the upper electrode film 410 by sputtering method (Col. 23, Lines 27-41).

And also teaches a specific example, in Fig. 24 and related text, wherein the lower gate electrode made of tantalum has a thickness of 200nm and is covered by the upper gate electrode made of aluminum alloy that has a thickness of 150nm (Col. 26, Lines 41-44).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the layer of conductive material (upper gate) by depositing the layer of conductive material in a non-conformal layer by sputtering as a metallic layer of Takehashi to have a thickness less than that of the gate (lower gate) as such does not produce unexpected results from what is taught in the prior art and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Referring to Claim 13, Takehashi teaches a method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate (42) separated from a polycrystalline silicon layer (1) by an insulating layer (2) (Fig. 12e and 12f);

(b) implanting a dopant (P+) into the polycrystalline silicon layer (1) using the gate (42) as a mask (Fig. 12g);

(c) forming a spacer layer (43) after step (b) adjacent to the gate (42) that comprises a conductive region which overlies the polycrystalline silicon layer (1) and extends along the gate (42) side wall, comprising depositing a layer of conductive material (430) over the polycrystalline silicon layer (1) and the gate (42), and selectively etching the deposited layer of conductive material (430) to form the spacer (43) with a first portion overlying the polycrystalline silicon layer (1) and a second portion extending along on the side wall of the gate (42);

(d) implanting a dopant into the polycrystalline silicon layer (1) using the gate (42) and the spacer (43) as a mask to form a source or drain region (150 and 160), such that the spacer (43) overlies an LDD region (152 and 162) in the polycrystalline silicon layer (1) between the source or drain region and the channel (170).

Though not explained in detail in this particular embodiment, Takehashi makes clear with regard to other embodiments of forming the layer of conductive material (upper gate electrode) wherein the selective etching of the conductive layer is carried out by standard photolithography known in the art and shown in Fig. 19(d) for example, by forming a mask (13) over the first portion thereof, and selectively etching the conductive layer (upper gate) where not protected by the mask (13) as is the standard in the art. The mask constitutes the fillet required to pattern the layer of conductive material (430) to form the spacer layer (upper gate electrode; 43).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to selectively etch the layer of conductive material (430) of the embodiment shown in Fig. 12(h) by forming a fillet (mask) over the first portion

thereof, and selectively etching the layer of conductive material where not protected by the fillet (mask) as such is a well known and established process in the art for removing portions of conductive material leaving only the pertinent portion as shown in Fig. 13(i) and would not produce a new and unexpected result.

Referring to Claim 9, Takehashi teaches all of the limitations but does not explicitly state in this embodiment wherein the layer of conductive material (43) has a thickness less than that of the gate (42). However, Takehashi teaches:

> Regarding the material of the two-staged gate electrode, the density of the material of the upper gate electrode 42 is desired to be higher than that of the lower gate electrode 43 from the standpoint of the height of gate electrode (if too high, however, such inconvenience would arise as too thick a gate insulator) and masking effect. More concretely, the material of the lower gate electrode 42 will preferably be Al, Al/Ti, Al/Zr/Ti, while that of the upper gate electrode 43 will preferably be Ta, Cr, Mo, etc (Col. 18, Lines 55-63).
>
> As has been described earlier, the density of the material for the upper gate electrode should be higher than that for the lower gate electrode in due consideration of the necessity of perfect masking capacity at the time of the second doping (Col. 20, Lines 10-13).
>
> The upper gate electrode film 420 was made to accumulate on the SiO.sub.2 film. Although this embodiment used the ITO film as shaped by sputtering method (film thickness: about 500Å), we may safely use such metallic films as aluminum, tantalum, titanium, molybdenum, tungsten, and zirconium, their alloy-based films, and such conductive oxide films as ITO. In these cases, however, the optimal film thickness should be determined individually in due consideration of the doping in the LDD area using this lower electrode as mask in the subsequent process. Further, since the stopping power of the ions (capacity to interfere with the passing of accelerated ions) to be doped depends on the film material, the optimal film thickness is naturally dependent also on the material composition of the film. (c) Formed on the lower gate electrode film 420 was a tantalum film of 2000 Å in thickness as the upper electrode film 410 by sputtering method (Col. 23, Lines 27-41).

And also teaches a specific example, in Fig. 24 and related text, wherein the lower gate electrode made of tantalum has a thickness of 200nm and is covered by the upper gate electrode made of aluminum alloy that has a thickness of 150nm (Col. 26, Lines 41-44).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the layer of conductive material (upper gate) by depositing the layer of conductive material in a non-conformal layer by sputtering as a metallic layer of Takehashi to have a thickness less than that of the gate (lower gate) as such does not produce unexpected results from what is taught in the prior art and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Allowable Subject Matter

Claims 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

/DAVID VU/
Primary Examiner, Art Unit 2818